UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

FORM 8-K

CURRENT REPORT
Pursuant to Section 13 or 15(d) of the Securities Exchange Act of 1934

Date of Report (Date of earliest event reported): August 29, 2022

Camber Energy, Inc.

(Exact name of registrant as specified in its charter)

Nevada	**000-29219**	**20-2660243**
(State or other jurisdiction of incorporation)	(Commission File Number)	(IRS Employer Identification Number)

15915 Katy Freeway Suite 450, Houston, Texas	**77094**
(Address of principal executive offices)	(Zip Code)

Registrant's telephone number, including area code: **(281) 404-4387**

Not applicable.
(Former name or former address, if changed since last report)

Check the appropriate box below if the Form 8-K filing is intended to simultaneously satisfy the filing obligation of the registrant under any of the following provisions (see General Instructions A.2. below):

☐ Written communications pursuant to Rule 425 under the Securities Act (17 CFR 230.425)

☐ Soliciting material pursuant to Rule 14a-12 under the Exchange Act (17 CFR 240.14a-12)

☐ Pre-commencement communications pursuant to Rule 14d-2(b) under the Exchange Act (17 CFR 240.14d-2(b))

☐ Pre-commencement communications pursuant to Rule 13e-4(c) under the Exchange Act (17 CFR 240.13e-4(c)) Securities registered pursuant to Section 12(b) of the Act: None.

Title of each class	**Trading Symbol(s)**	**Name of each exchange on which registered**
Common Stock	**CEI**	**NYSE American**

Indicate by check mark whether the registrant is an emerging growth company as defined in Rule 405 of the Securities Act of 1933 (§230.405 of this chapter) or Rule 12b-2 of the Securities Exchange Act of 1934 (§240.12b-2 of this chapter). ☐

If an emerging growth company, indicate by check mark if the registrant has elected not to use the extended transition period for complying with any new or revised financial accounting standards provided pursuant to Section 13(a) of the Exchange Act. ☐

Item 7.01. Regulation FD Disclosure.

Camber Energy, Inc. (the "Company") owns the majority of the issued and outstanding shares of common stock of Viking Energy Group, Inc. ("Viking"). Viking Protection Systems, LLC ("Viking Projection") is a majority-owned subsidiary of Viking.

Viking Protection engaged Nayak Corporation, a third-party power systems engineering company ("Nayak"), to test Viking Protection's open conductor detection technology, based on a testing plan prepared by Viking Protection's engineering team with input from a company that manufactures protective relay devices in which the technology may be incorporated. Nayak issued the report with testing results furnished herewith as Exhibit 99.1, which is incorporated by reference into this Item 7.01. Sections of the report containing confidential information have been redacted.

The information contained in this Item 7.01 is being furnished and shall not be deemed "filed" for purposes of Section 18 of the Securities Exchange Act of 1934, as amended (the "Exchange Act"), or otherwise subject to the liabilities under Section 18 and shall not be deemed to be incorporated by reference into the filings of the Company under the Securities Act of 1933, as amended, or the Exchange Act.

Item 9.01. Financial Statements and Exhibits.

The exhibits listed in the following Exhibit Index are filed as part of this report:

Exhibit No.	Description
99.1	Report of Nayak Corporation dated August 29, 2022 (with redactions)
104	Cover Page Interactive Data File (embedded within Inline XBRL document)

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned hereunto duly authorized.

CAMBER ENERGY, INC.

Date: August 31, 2022

By: */s/ James A. Doris*
Name: James A. Doris
Title: Chief Executive Officer

RTDS CHIL Testing Results of Viking Open Conductor Detection Scheme Using a Competitive Relay – Phase II

For
Viking Protection Systems

Prepared by:

[redacted]

Reviewed by:

[redacted]
8/29/2022

Revision 1: **8/29/2022**

Nayak Corporation
23 Orchard Rd., Ste. 202
Skillman, NJ 08558

www.nayakcorp.com
info@nayakcorp.com

Legal Notice

This report was prepared by Nayak for Viking Protection Systems. Neither Nayak nor any person acting on its behalf:

1. makes any warranty or representation, expressed or implied, with respect to the use of any information contained in this report, or that the use of any information, apparatus, method, or process disclosed in the report may not infringe privately owned rights.

2. assumes any liabilities with respect to the use of or for damage resulting from the use of any information, apparatus, method, or process disclosed in this document.

Table of Contents

Revision notes
Revision 0 – 8/13/2022 Revision 1 – **8/29/2022**
Editorial changes, reorganizing of Summary section

1 Introduction

The open conductor situation of transmission lines is of significant concern to transmission and distribution utilities, since it can lead to wildfire and other similar issues. The conventional line protection systems currently in use are not designed to detect this condition.

The Viking Protection Systems have developed a proprietary concept for detecting the open conductor situation of transmission lines. This algorithm uses the off-the-shelf protective relays. Nayak has supported Viking to perform hardware in loop (HIL) testing of these relays to help Viking evaluate the effectiveness of their concept. In Phase I of this project, the concept was tested on the line differential relays. That test was not conclusive, for details, please refer to the Phase I report. However, Viking gained valuable information from the relay tests and Phase II tests were performed using competitive relays. This document describes the CHIL testing of competitive relays using the RTDS™ real-time digital simulator.

2 Assumptions

- The transmission lines' zero-sequence impedances are assumed to be four times the positive sequence value.
- Bus source impedance is assumed to be 0.03315728 H.

3 Methodology

This section provides the details of the RSCAD model development of the proposed test network that was supplied to Nayak by Viking.

3.1 RSCAD Model Development

The test network provided by Viking is shown in Figure 1. It was modeled in RSCAD FX V 1.1 by importing the provided PSSE V33 .raw file into RSAD using the RSCAD's PSSE file import tool. The entire network in the raw file was imported. It was assumed that the provided .raw file has the proper boundary equivalent sources with appropriate short circuit impedances. This network includes the following 500 kV, 230 kV, and 115 kV transmission lines:

- 500kV Line 1
- 500kV Line 2
- 500 kV Line 3
- 500 kV Line 4
- 500 kV Line 5
- 230kV Line 1
- 230kV Line 2
- 115kV Line 1
- 115kV Line 2

The imported case only contains the positive sequence values of the transmission line parameters. Since the study is focused on open conductor detection, it is crucial to model the zero-sequence data of the network. As per Viking, the zero-sequence impedance values were assumed as four times positive sequence impedance. The converted transmission line model parameters were modified to include the zero sequence values based on this assumption.

The developed model in RSCAD was validated to ensure that the data in the RSCAD model is correct. The validation was performed by comparing the RSCAD steady-state results against the load flow and short circuit results as follows:

- The active and reactive power flow values in the lines and equivalent sources and the bus voltage magnitude and angle of the RSCAD were compared with the PSSE load flow results.
- The values for fault currents of RSCAD were compared against the PSSE short-circuit results for 3-phase-G.

Up to 10% error between the two software simulation results is acceptable based on the industry experience and practices. But when performing the comparison, the absolute value was also considered in addition to the percentage value since small differences between small values (line flows) must be acceptable even though they may amount to large percentage mismatch.

Figure 1: The phase II test network in RTDS

3.2 HIL Setup

The validated model was modified to include the hardware relays at the sending and receiving end of the designated transmission line for validating open conductor simulation. The case was modified to perform the conventional relay testing with analog measurements. Analog output channels (RTDS GTAO card) were used to send the voltage and current measurement from the RTDS simulations to the relays, while GTFPI card was used to send breaker status and receive relay trip signals. RTDS GTAO signals are low-level signals in the range of $\pm$ 10V. But the relays expect the voltage and current as output from the PTs and CTs. Hence, a Doble F6350e was used to amplify the RTDS GTAO outputs as expected by relays.

The corresponding software GTAO and GTFPI components were added to the validated RSCAD model. The scaling of the GTAO was adjusted based on the relay's CT/PT scaling and amplifier gains. A single competitive relay configured with the Viking algorithm was used as protective relay at one end of the line. The relay was fed the voltage and current from either end of the line through GTAO and Doble amplifier interface.

The hardware-in-loop testing process consists of the following steps:

1. Test the output signals from the GTAO card to ensure its output for nominal voltage/current is within the expected range. This test was done using a multimeter.
2. Connect GTAO outputs to the amplifier input.
3. Monitor the amplifier outputs (voltage and current) before connecting to the relay inputs.
4. Connect the amplifier output to relay input.
5. Verify that the primary side measurement on the relay matches that in RTDS to ensure proper scaling and connection.
6. Manually test to check the proper connection and for preliminary verification of settings.
7. Execute the test plan simulations and collect the simulation results.

3.2.1 Inputs to RTDS

1. Breaker trip signals from the relays through GTFPI digital inputs.

3.2.2 Outputs from RTDS

1. Instantaneous voltages (6 channels) and currents (6 channels) at both ends of the line through RTDS GTAO cards to Doble F6350e, which amplifies the RTDS outputs.
2. The breaker open/close status through GTFPI. The relay requires a 125V DC signal to receive a breaker close status. Hence, the GTFPI HV panel was used. The 125V dc vetting source was provided by Doble amplifier's battery simulation output. While this status was wired back to the relay in Phase I, it was connected back to the competitive relay as Viking did not ask for it.

3.2.3 RTDS Case Setup for the Hardware Interface

The measurements are scaled as shown in Figure 2 and provided to the GTAO, which provides the signals to the amplifier.

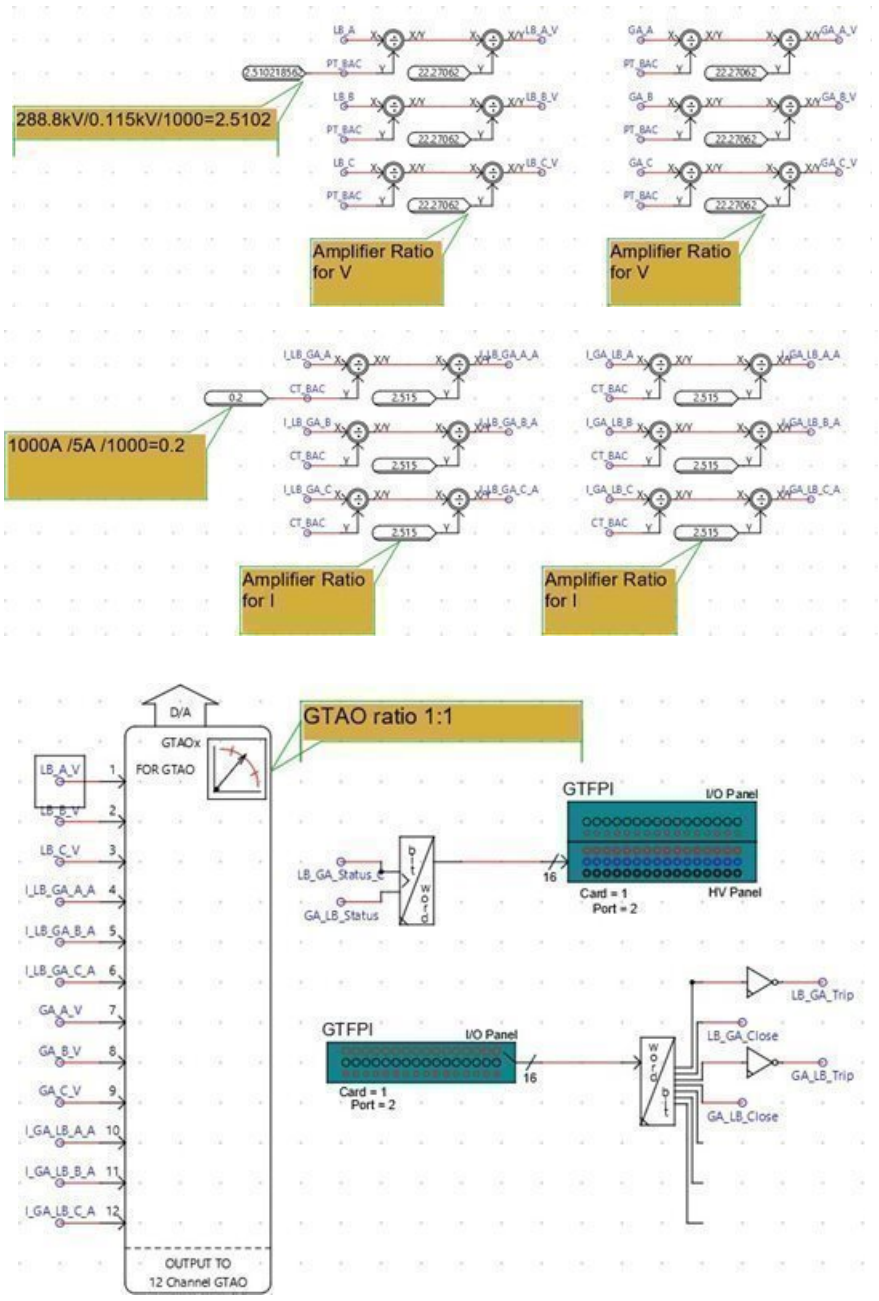

Figure 2: Analog and Digital I/O

3.3 RTDS Test Plan

RTDS case was set up to perform tests as per the test plan provided by Viking. Simulation results are discussed in the following section.

4 RTDS CHIL Test Results

4.1 Testing the relay connections

To validate the HIL connection, the competitive relay readings of grid voltage and line currents were compared with the measurements in the RTDS. Similar comparisons were made for other relevant quantities such as differential currents, charging currents, positive sequence magnitude, angle, etc. All these quantities measured in the relay matched the corresponding measurements in the RTDS. Hence, it was established that the relay connections are correct. Manual trip and reset of the relays were performed to confirm the correct operation of trip signal.

4.2 HIL Testing of the competitive relays

HIL simulations were performed with the competitive relay programmed by Viking representatives present on site. Not all lines were tested for full range of length, loading, and faults. Tests in Phase II (this report) were done as per requests from Viking team in the lab. They are a subset of the test plan. This section summarizes the RTDS HIL simulation results. Please note that this document contains only the results captured from RSCAD (RTDS GUI) and does not contain any test results from within the relay. The only information from the relay that was captured in the RSCAD is the trip signal (0 or 1) issued by the relay. RTDS test setup treats the relay as a black box that receives voltages and currents as inputs from the RTDS and sends back a trip signal to the RTDS. Hence, the trip signal captured in the RSCAD does not provide any internal information about the relay such as which individual element(s) in the relay issued the trip signal, relay setting parameters, etc. Because the trip signal plots in RSCAD are synchronized with the events (faults, opening of the conductor, etc.), those plots will show relative time between the event and the trip. Some initial tests did not include trip signals.

4.2.1 500 kV line tests

A 500 kV line is chosen as the line to be tested for 500 kV testing

4.2.1.1 Steady state values for different loading conditions:

4.2.1.1.1 500kV System: Close to 0% loading (0.1 MW and 0.1MVAR at the 500kV bus)

Figure 3: Current Plots: Plots removed for patent pending protection.

Figure 4: Sequence current plots: Plots removed for patent pending protection.

4.2.1.1.2 500kV System: Close to 50% loading (1500 MW and 50MVAR at the 500kV bus)

Figure 5: Plots removed for patent pending protection.

Figure 6: Sequence current plots: Plots removed for patent pending protection.

4.2.1.1.3 500kV System: Close to 95% loading (2850 MW and 95MVAR at the 500kV bus)

Figure 7: Current Plots: Plots removed for patent pending protection.

Figure 8: Sequence current plots: Plots removed for patent pending protection.

4.2.1.2 Tests performed on Jul 27 2022

Note: Only 500kV configuration was tested and the Trip signal connection to RTDS was not established

4.2.1.2.1 1: Open conductor phase A at 50%line length with 0.1MW and 0.1MVAR loading

Figure 9: Current plots for test 1: Plots removed for patent pending protection.

Figure 10: Sequence current plots for test 1: Plots removed for patent pending protection.

4.2.1.2.2 2: AG Fault in the same line at 50%line length with 0.1MW and 0.1MVAR loading (AG fault for 10 Cycles)

Figure 11: Current plots for test 2: Plots removed for patent pending protection.

Figure 12: Sequence current plots for test 2: Plots removed for patent pending protection.

4.2.1.2.3 3: AB fault in the same line at 50%line length with 0.1MW and 0.1MVAR loading (AB fault for 10 Cycles)

Figure 13: Current plots for test 3: Plots removed for patent pending protection.

Figure 14: Sequence current plots for test 3: Plots removed for patent pending protection.

4.2.1.2.4 4: ABG fault in the same line at 50%line length with 0.1MW and 0.1MVAR loading (ABG fault for 10 Cycles)

Figure 15: Current plots for test 4: Plots removed for patent pending protection.

Figure 16: Sequence current plots for test 4: Plots removed for patent pending protection.

4.2.1.2.5 5: Open conductor phase A at 50%line length with 50%loading (1500MW and 50 MVAR)

Figure 17: Current plots for test 5: Plots removed for patent pending protection.

Figure 18: Sequence current plots for test 5: Plots removed for patent pending protection.

4.2.1.2.6 6: Open conductor phase A at 50%line length with 95%loading (2850MW and 95 MVAR)

Figure 19: Current plots for test 6: 1. Plots removed for patent pending protection.

Figure 20: Sequence current plots for test 6: Plots removed for patent pending protection.

4.2.1.2.7 7: Open conductor phase A at 50%line length with 95%loading (2850MW and 95 MVAR) AG Fault

Figure 21: Current plots for test 7: Plots removed for patent pending protection.

Figure 22: Sequence current plots for test 7: Plots removed for patent pending protection.

4.2.1.2.8 8: AB Fault at 50%line length with 95%loading (2850MW and 95 MVAR)

Figure 23: Current plots for test 8: Plots removed for patent pending protection.

Figure 24: Sequence current plots for test 8: Plots removed for patent pending protection.

4.2.1.2.9 9: ABG Fault at 50%line length with 95%loading (2850MW and 95 MVAR)

Figure 25: Current plots for test 9: Plots removed for patent pending protection.

Figure 26: Sequence current plots for test 9: Plots removed for patent pending protection.

4.2.1.2.10 10: AG Fault at line distance 30% from the bus with 95%loading (2850MW and 95 MVAR)

Figure 27: Current plots for test 10: Plots removed for patent pending protection.

Figure 28: Sequence current plots for test 10: Plots removed for patent pending protection.

4.2.1.2.11 11: AB Fault at line distance 30% from the bus with 95%loading (2850MW and 95 MVAR)

Figure 29: Current plots for test 11: Plots removed for patent pending protection.

Figure 30: Sequence current plots for test 11: Plots removed for patent pending protection.

4.2.1.2.12 12: ABG Fault at line distance 30% from the bus with 95%loading (2850MW and 95 MVAR)

Figure 31: Current plots for test 12: Plots removed for patent pending protection.

Figure 32: Sequence current plots for test 12: Plots removed for patent pending protection.

4.2.1.3 Tests performed on Jul 29, 2022

Note: Only 500kV, 115kV (initial test) configuration was tested and the Trip signal connection to RTDS is established.

4.2.1.3.1 13: Open conductor phase A at 50%line length with 50% loading 1500MW and 50MVAR loading

Figure 33: Current plots for test 13: Plots removed for patent pending protection.

Figure 34: Sequence current plots for test 13: Plots removed for patent pending protection.

4.2.1.3.2 14: Open conductor phase A at 50%line length with 95% loading 2850MW and 95MVAR loading

Figure 35: Current plots for test 14: Plots removed for patent pending protection.

Figure 36: Sequence current plots for test 14: Plots removed for patent pending protection.

4.2.1.3.3 15: AG Fault at 50%line length with 95%loading (2850MW and 95 MVAR)

Figure 37: Current plots for test 15: Plots removed for patent pending protection.

Figure 38: Sequence current plots for test 15: Plots removed for patent pending protection.

4.2.1.3.4 16: Open conductor phase A at 10%line length with 95%loading (2850MW and 95 MVAR)

Figure 39: Current plots for test 16: Plots removed for patent pending protection.

Figure 40: Sequence current plots for test 16: Plots removed for patent pending protection.

4.2.1.3.5 17: Open conductor phase A at 80%line length with 95%loading (2850MW and 95 MVAR)

Figure 41: Current plots for test 17: Plots removed for patent pending protection.

Figure 42: Sequence current plots for test 17: Plots removed for patent pending protection.

4.2.2 230kV line tests

4.2.2.1 Steady state values for different loading conditions

4.2.2.1.1 230kV System: Close to 100% loading (600 MW and 100MVAR at the 1 230kV bus)

Figure 43: Current Plots: Plots removed for patent pending protection.

Figure 44: Sequence current plots: Plots removed for patent pending protection.

4.2.2.2 Tests performed on Jul 30, 2022

4.2.2.2.1 18: Open conductor phase A at 50%line length with 100%loading (600MW and 100 MVAR)

Figure 45: Current Plots for test 18: Plots removed for patent pending protection.

Figure 46: Sequence current plots for test 18: Plots removed for patent pending protection.

4.2.2.2.2 19: Open conductor phase A at 10%line length with 100%loading (600MW and 100 MVAR)

Figure 47: Current Plots for test 19: Plots removed for patent pending protection.

Figure 48: Sequence current plots for test 19: Plots removed for patent pending protection.

4.2.2.2.3 20: Open conductor phase A at 75%line length with 100%loading (600MW and 100 MVAR)

Figure 49: Current Plots for test 20: Plots removed for patent pending protection.

Figure 50: Sequence current plots for test 20: Plots removed for patent pending protection.

4.2.2.2.4 21: AG Fault at 75%line length of PAN GA 2 with 100%loading (600MW and 100 MVAR)

Figure 51: Current Plots for test 21: Plots removed for patent pending protection.

Figure 52: Sequence current plots for test 21: Plots removed for patent pending protection.

4.2.2.2.5 22: ABG Fault at 75%line length of PAN GA 2 with 100%loading (600MW and 100 MVAR)

Figure 53: Current Plots for test 22: Plots removed for patent pending protection.

Figure 54: Sequence current plots for test 22: Plots removed for patent pending protection.

4.2.2.2.6 23: AB Fault at 75%line length of PAN GA 2 with 100%loading (600MW and 100 MVAR)

Figure 55: Current Plots for test 23: Plots removed for patent pending protection.

Figure 56: Sequence current plots for test 23: Plots removed for patent pending protection.

4.2.2.2.7 24: AG Fault at 75%line length of PAN GA 1 with 100%loading (600MW and 100 MVAR)

Figure 57: Current Plots for test 23: Plots removed for patent pending protection.

Figure 58: Sequence current plots for test 23: Plots removed for patent pending protection.

4.2.3 115kV line tests

4.2.3.1 Steady state values for different loading conditions:

4.2.3.1.1 115kV System: Close to 25% loading (50 MW and 5MVAR at the 115kV bus)

Figure 59: Current Plots: Plots removed for patent pending protection.

Figure 60: Sequence current plots: Plots removed for patent pending protection.

4.2.3.2 Tests performed on Jul 29, 2022

Testing the initial setting for the 115kV configuration

4.2.3.2.1 25: Open conductor phase A at 100%line length with 25%loading (50MW and 5 MVAR)

Figure 61: Current Plots for test 25: Plots removed for patent pending protection.

Figure 62: Sequence current plots for test 25: Plots removed for patent pending protection.

4.2.3.3 Tests performed on Jul 30, 2022

4.2.3.3.1 26: Open conductor phase A at 100%line length with 25%loading (50MW and 5 MVAR)

Figure 63: Current Plots for test 26: Plots removed for patent pending protection.

Figure 64: Sequence current plots for test 26: Plots removed for patent pending protection.

4.2.3.3.2 27: Open conductor phase A at 50%line length with 25%loading (50MW and 5 MVAR)

Plots removed for patent pending protection.

Figure 65: Current Plots for test 27: Plots removed for patent pending protection.

Figure 66: Sequence current plots for test 27: Plots removed for patent pending protection.

4.2.4 70kV line tests

4.2.4.1 Steady state values for different loading conditions:

4.2.4.1.1 70kV System: Close to 100% loading (20 MW and 5MVAR at the VDSB 1 70kV bus)

Figure 67: Current Plots: 1. Plots removed for patent pending protection.

Figure 68: Sequence current plots: Plots removed for patent pending protection.

4.2.4.1.2 70kV System: Close to 30% loading (6 MW and 2 MVAR at the VDSB 1 70kV bus)

Figure 69: Current Plots: Plots removed for patent pending protection.

Figure 70: Sequence current plots: Plots removed for patent pending protection.

4.2.4.1.3 70kV System: Close to 0% loading (0.1 MW and 0.1 MVAR at the VDSB 1 70kV bus)

Figure 71: Current Plots: Plots removed for patent pending protection.

Figure 72: Sequence current plots: Plots removed for patent pending protection.

4.2.4.2 Tests performed on Jul 30, 2022

4.2.4.2.1 28: Open conductor phase A at 50%line length with 100%loading (20MW and 5 MVAR)

Figure 73: Current Plots for test 28: Plots removed for patent pending protection.

Figure 74: Sequence current plots for test 28: Plots removed for patent pending protection.

4.2.4.2.2 29: Open conductor phase A at 50%line length with 30%loading (6MW and 2 MVAR)

Figure 75: Current Plots for test 29: Plots removed for patent pending protection.

Figure 76: Sequence current plots for test 29: Plots removed for patent pending protection.

4.2.4.2.3 30: Open conductor phase A at 50%line length with 0%loading (0.1MW and 0.1 MVAR)

Figure 77: Current Plots for test 30: Plots removed for patent pending protection.

Figure 78: Sequence current plots for test 30: Plots removed for patent pending protection.

5 Summary

This report presents the RTDS CHIL testing results of competitive relay programmed by Viking with their open conductor detection logic. Testing was done on several lines of 4 different voltage levels. The trip signal reported in the plot is the output of a latch which is triggered by the first rising edge of the input trip signal coming into the RTDS from the relay. Because of the limited time available for tests, only selective tests from the test plan that were requested by Viking team were performed and those are the tests reported here. The plots are all self-explanatory with their detailed heading and captions for the figures. Following is the summary of the test results:

- **Open conductor**: The relay tripped on all open conductor events tested except for one test on 70kV line under low load condition Tests conducted are grouped into their respective voltage classes and are summarized below:
    - 500 kV lines: Tripped on all open conductor events tested. The type of tests in this category were the most exhaustive compared to the tests in other voltage class lines. Tests ranged for different lengths (5% - 95%) and different loading (0% -100%).
    - 230 kV lines: Tripped on all open conductor events tested. Only 3 tests were conducted, and all were 100% loading. No 0% load tests were done.
    - 115 kV lines: Tripped on all open conductor events tested. Only 3 tests were conducted, and all were with 25% loading. No 0% load tests were done.
    - 70 kV lines: Only 3 tests were conducted. Relay tripped on 100% and 30% loading tests but did not trip for low (nearly 0%) loading. There was significant chatter on input trip signal coming into the RTDS from the relay for all 70 kV events. The trip signal in the report is a latched signal with the chattering behavior cleaned.
- **Faults**: The relay did not trip on any faults studied
    - Not all faults were applied to all lines
    - No faults were studies for 115kV and 70kV lines

Note: Nayak only observed the trip signal received from the relay and did not have any information about any internal workings of the relays such as which element of the relay picked up during an event if there were multiple active elements. Further details of such an operation can only be provided by Viking.